ANUP CHAKAR

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SUMMARY *[**NOTE:** These 3-4 bullet points must be customized to the job ad]*

- 5 years of combined research and engineering experience in processor and SoC architectures, performance modeling and benchmarking
- Strong focus on evaluation and analysis of processor architectures, memory subsystem microarchitectures, and system issues cross-cutting hardware-software-OS levels
- Experienced in working with global teams including senior architects, marketing based in US, India, Israel

SKILLS

C/C++, Verilog, VHDL, Perl, Shell scripting, Matlab, CVS, ClearCase, Linux, Embedded Linux (ELDK), Uboot, Assembly language (PowerPC, MIPS, 8051), Synopsys Design Compiler, Oprofile, Linux kernel instrumentation

EDUCATION

University of California, Irvine | **PhD in Computer Science** Aug 20XX
Indian Institute of Technology [IIT], Bombay, India | **M.Tech in Electronic Systems** Mar 20XX
College of Engineering, India | **BE(Hons) in Electronics & Instrumentation Engineering** Jun 20XX

RESEARCH EXPERIENCE

Graduate Researcher, Center for Embedded Computing Systems, UC Irvine Sep 20XX – Present
Research in Error, Power, Temperature-Aware Embedded Architectures

- Coordinated several research projects on single-core and multi-core embedded architectures which are error- resilient and aware of power and thermal conditions
- Advanced micro-architecture of a highly reliable Data Cache which is resilient of process-variation induced errors in SRAM arrays
- Computed a methodology to analyze memory access trace of applications
- Experiment with machine-learning techniques to extract information from memory access patterns and use such information in customizing memory architectures

PROFESSIONAL EXPERIENCE

Co-founder, SIMON, San Diego, CA Dec 20XX – Present

- Co-founded the concept of SIMON, a revolutionary new watch that promotes cardiovascular fitness by monitoring and recording heart rate and activity and providing suggestions to improve one's health
- Co-developed a business plan with marketing, medicine and engineering professionals and students
- Winner of 3rd place in 20XX Business Plan Competition at Paul Merage School of Business resulting in Seed Financing Invitation from Tech Coast Angels, California

Engineering Intern, Freescale Semiconductors, Austin, TX Jun 20XX – Sep 20XX
Performance Analysis of PowerPC based systems for Storage Market

- Characterized and analyzed performance of a processor targeted towards disk-attached and network-attached storage systems (DAS and NAS). Directly impacted Freescale's marketing efforts favorably
- Developed a complete analysis methodology using microbenchmarks, tests and standard storage benchmarks to identify performance bottlenecks in NAS/DAS systems with multiple hardware-software components (OS, Ethernet, SATA)
- Performance analysis of multicore QorIQ processor using Simics system simulator and Freescale's internal performance models

PROFESSIONAL EXPERIENCE, CONT'D

Design Engineer II, Freescale Semiconductors, India May 20XX – August 20XX

Architecture Analysis of PowerPC Processors

- Analysis of architecture performance for several PowerPC cores (e500, e300) using cycle accurate simulators
- Workload analysis for SPEC CPU, EEMBC and customer applications and developed key insights about effectiveness of various architectural features in PowerPC superscalar core, caches and SoCs
- Development of Architecture Performance Models (cycle-accurate and transaction-level models) for PowerPC cores and SoCs
- Compiler flag mining to characterize the effects of GreenHills compiler flags on embedded benchmarks

Development of a software energy profiler for StarCore VLIW DSP

- Development of an accurate power model integrated with a fast ISS of the StarCore DSP platform for software developers to obtain a function-wise energy cost profile of software applications
- Established a large suite of DSP benchmarks like filters, FFT, codecs and control codes for testing and validating the energy model.
- Conducted a case study demonstrating the potential for software energy optimization using ITU- T G.729 speech codec application
- Communicated scientific findings via conference presentations and resulting in best paper award in Freescale Technical Symposium 20XX

Associate Software Engineer, ST Microelectronics, India Aug 20XX -- May 20XX

Development of physical layer software for 3G basestations

- Development of Inner and Outer Modem software on ST140 based DSP platforms for 3G cellular network base stations for WCDMA, CDMA2000 and EDGE standards
- Evaluated several DSP modules such as channel estimation, path search and automatic frequency correction for CDMA rake receiver as well as convolutional coder, Viterbi and Turbo decoders for various wireless standards

ACADEMIC PROJECTS

Indian Institute of Technology [IIT], Bombay October 20XX

Design and Implementation of DSP-based Multiprocessing System for Real Time Simulations

- Design and development of a multiprocessor-based system to perform Hardware-in-Loop Real Time Simulations
- Remodeled novel inter-processor bus architecture for a scalable multiprocessor system using to enable inter- processor communication in a consistent and predictable time

AWARDS AND HONORS

- 3rd position in 20XX Business Plan Competition, Paul Merage School of Business at UC Irvine, June 20XX
- Young Engineering Fellowship, Indian Institute of Science, Bangalore, May 20XX
- University Gold Medalist for first rank in Bachelor of Engineering program, College of Engineering and Management, India, June 20XX
- Best Paper Award in Freescale Technical Symposium, New Delhi, March 20XX