# ANUP CHAKAR

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## SUMMARY

- 5 years of combined research and engineering experience in processor and SoC architectures, performance modeling and benchmarking.
- Strong focus on evaluation and analysis of processor architectures, memory subsystem microarchitectures, and system issues cross-cutting hardware-software-OS levels. Experienced in working on PowerPC, StarCore VLIW DSP, ST140 DSP architectures.
- Good application knowledge and development experience in embedded, signal processing including 3G wireless.
- Experienced in working with global teams including senior architects, marketing based in US, India, Israel.

### Computer Skills, Tools and Programming Languages

- C/C++, Verilog, VHDL, Perl, Shell scripting, Matlab, CVS, ClearCase, Linux, Embedded Linux (ELDK), Uboot, Assembly language (PowerPC, MIPS, 8051), Synopsys Design Compiler, Oprofile, Linux kernel instrumentation**.**

## EDUCATION

- **University of California, Irvine** *Phd in Computer Science (currently pursuing)*
- **Indian Institute of Technology [IIT], Bombay, India** *M.Tech in Electronic Systems*, 20XX-20XX
- **College of Engineering and Management, India** *BE(Hons) in Electronics & Instrumentation Engg*, 20XX-20XX, Graduated with University Gold Medal

## WORK EXPERIENCE

### Co-founder, SIMON (Dec 20XX – Present)

- Co-founded the concept of SIMON, a revolutionary new watch that promotes cardiovascular fitness by monitoring and recording one's heart rate and activity and providing helpful suggestions to improve one's health.
- Co-developed a business plan with Marketing, Medicine and Engineering professionals and students. Winner of 3rd place in 20XX Business Plan Competition at Paul Merage School of Business. Received Seed Financing Invitation from Tech Coast Angels, California.

### Graduate Researcher, Center for Embedded Computing Systems, University of California, Irvine (Sep 20XX – Present)

***Research in Error, Power, Temperature-Aware Embedded Architectures***

- Working on several research projects on single-core and multi-core embedded architectures which are error-resilient and aware of power and thermal conditions.
- Developing the micro-architecture of a highly reliable Data Cache which is resilient of process-variation induced errors in SRAM arrays.
- Developing a methodology to analyze memory access trace of applications. Experimenting with machine-learning techniques to extract information from memory access patterns and use such information in customizing memory architectures.

### Intern, Freescale Semiconductors, Austin (June 20XX – Sep 20XX)

***Performance Analysis of PowerPC based systems for Storage Market***

- Characterized and analyzed performance of a processor targeted towards disk-attached and network-attached storage systems (DAS and NAS). Directly impacted Freescale's marketing efforts favorably.
- Developed a complete analysis methodology using microbenchmarks, tests and standard storage benchmarks to identify performance bottlenecks in NAS/DAS systems with multiple hardware-software components (OS, Ethernet, SATA).
- Performance analysis of multicore QorIQ processor using Simics system simulator and Freescale's internal performance models.

**Design Engineer II, Freescale Semiconductors, India (May 20XX – August 20XX)**
***Architecture Analysis of PowerPC Processors***

- Architecture performance analysis for several PowerPC cores (e500, e300) using cycle accurate simulators. Workload analysis for SPEC CPU, EEMBC and customer applications. Developed key insights about effectiveness of various architectural features in PowerPC superscalar core, caches and SoCs.
- Development of Architecture Performance Models (cycle-accurate and transaction-level models) for PowerPC cores and SoCs.
- Compiler flag mining to characterize the effects of GreenHills compiler flags on embedded benchmarks.

***Development of a software energy profiler for StarCore VLIW DSP***

- Development of an accurate power model integrated with a fast ISS of the StarCore DSP platform. The model was developed for software developers to obtain a function-wise energy cost profile of software applications.
- Developed a large suite of DSP benchmarks like filters, FFT, codecs and control codes for testing and validating the energy model. Conducted a case study demonstrating the potential for software energy optimization using ITU-T G.729 speech codec application.
- Resulted in a publication in 20XX International VLSI Design Conference and best paper award in Freescale Technical Symposium 20XX

**Associate Software Engineer, ST Microelectronics, India (Aug 20XX -- May 20XX)**
***Development of physical layer software for 3G basestations***

- Development of Inner and Outer Modem software on ST140 based DSP platforms for 3G cellular network base stations for WCDMA, CDMA2000 and EDGE standards. Developed several DSP modules such as channel estimation, path search and automatic frequency correction for CDMA rake receiver as well as convolutional coder, Viterbi and Turbo decoders for various wireless standards.

## PREVIOUS ACADEMIC WORK

**M.Tech Thesis**: **Design and Implementation of DSP-based Multiprocessing System for Real Time Simulations**

- Design and development of a multiprocessor based system to perform Hardware-in-Loop Real Time Simulations. Targeted applications were electric power systems and power electronic systems.
- Designed novel inter-processor bus architecture for a scalable multiprocessor system using to enable inter-processor communication in a consistent and predictable time.

**Other Projects**: In various other projects I have designed and developed the following:

- A microcontroller based Barcode Reader
- A microcontroller based ADPCM speech codec
- A Floating Point Unit for implementation in FPGA
- An ADPCM speech codec for implementation in FPGA

## AWARDS AND HONORS

- 3rd position in 20XX Business Plan Competition in Paul Merage School of Business at Univ. of California Irvine
- Awarded an Young Engineering Fellowship by Indian Institute of Science, Bangalore in May 20XX
- Won University Gold Medalist for first rank in Bachelor of Engineering program.
- Won the Best Paper Award in Freescale Technical Symposium, New Delhi in March 20XX